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EXAMINER
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BIRENBAUM, NIRA S

ART UNIT	PAPER NUMBER
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1742

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/769,605

Applicant(s)

UZOH ET AL.

Examiner

Nira S. Birenbaum, Ph.D.

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 01 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9-13 and 15-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☒ Claim(s) 1-20 are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 11-23-04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Restriction/Election*

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-7, 9-13 and 15-20, drawn to a method, classified in class 205, subclass 104.
- II. Claims 8 and 14, drawn to a product, classified in class 428, subclass 620.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made.

The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case a semiconductor device can be made using other plating techniques such DC plating without any pulsed deposition steps.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Tina Chen on October 3, 2005 a provisional election was made without traverse to prosecute the invention of I, claims 1-7, 9-13 and 15-20. Affirmation of this election must be made by applicant in replying to this Office action. Claims 8 and 14 are withdrawn from

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further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

#### ***Claim Objections***

Claim 7 is objected to because of the following informalities: Claim 7 should depend from claim 1, not claim 11. Appropriate correction is required.

#### ***Claim Interpretations***

Regarding the limitation in claim 15, where the second cavity is unfilled after forming the first conductive layer, the examiner would like to clarify the meaning of the word "unfilled". "Unfilled" can mean either "empty" or "partially full". It is the examiner's position that in this case, the word "unfilled" should be interpreted to mean "partially full".

Regarding the last limitation of claims 1, 9, and 15, where the second conductive layer has a planar portion over both cavities, it is the examiner's position that "planar" should be interpreted as "substantially planar", as recited in the preamble of each claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 5, 7, 9, 10, 15 – 18, and 20 are rejected under 35

U.S.C. 102(e) as being anticipated by Dubin *et al.* (US Patent No. 6,432,821) as evidenced by Uzoh *et al.* (US 2002/0061715).

Regarding claims 1, 9, and 15, Dubin *et al.* '821 teach a method for electrochemically filling cavities on a wafer surface comprising:

- applying a first cathodic current to form a conductive layer on the wafer surface (see Figure 7, element 706). The conductive layer is formed over a first and second cavity where the first cavity is smaller than the second cavity and both cavities are less than 10 microns in width (column 5, lines 11-27).
- treating the surface of the conductive layer by applying a pulsed current (see Figure 7, element 710)
- applying a second cathodic current to form a second conductive layer over both cavities.

Regarding claims 9 and 15, the first conductive layer would inherently fill the smaller cavities while leaving the larger cavities partially filled as evidenced by Uzoh *et al.*, because Uzoh *et al.* teach that when plating a wafer with different size cavities, the smaller cavities become filled before the larger cavities (paragraph 5). Regarding claim 1, the surface of the conductive layer over a filled cavity is inherently substantially planar, as evidenced by Uzoh *et al.* (Figure 1b).

Regarding claims 2, 17 and 18, Dubin *et al.* '821 teach that the step of treating comprises an anodic pulsed current (see Figure 7, element 710).

Regarding claim 4, Dubin *et al.* '821 teach that the advantage of their method is that the height of humps over small features is reduced (column 6, lines 47-49).

Regarding claims 5 and 10, Dubin *et al.* '821 teach that the cathodic current comprises a DC voltage (see Figure 7, element 706).

Regarding claim 7, Dubin *et al.* '821 teach that the steps of applying current and treating the surface are repeated until all cavities are filled (column 5, lines 39-60).

Regarding claim 16, Dubin *et al.* '821 teach that the step of applying the cathodic current includes a rectangular waveform (see Figure 7, element 706).

Regarding claim 20, Dubin *et al.* '821 teach that the conductive layer is copper (column 5, lines 4-11).

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 6, 11-13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin *et al.* '821 evidenced by Uzoh *et al.* as applied to claims 1, 9 and 15 above, and further in view of Dubin *et al.* (US Patent No. 5,972,192).

Dubin *et al.* '821 and Uzoh *et al.* teach the features as previously described. However, regarding claims 3 and 19, these references do not teach that the pulsed current comprises cathodic current.

Dubin *et al.* '192 teach a method for plating wafers comprising DC cathodic current followed by cathodic and anodic pulses, *i.e.*, forward-reverse pulse plating (example 3). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Dubin *et al.* '821 in view of Uzoh *et al.* by applying cathodic pulses as disclosed by Dubin *et al.* '192 because Dubin *et al.* '192 teach that forward-reverse pulse plating results in voidless filling of trenches with large-grain deposits (column 8, lines 45-50).

Regarding claims 6 and 11, Dubin *et al.* '821 and Uzoh *et al.* do not teach that the cathodic current comprises an AC waveform.

Dubin *et al.* '192 teach a method for plating wafers comprising forward-reverse pulsing (example 2). The forward (cathodic) pulses comprise an alternating cathodic current, which is then followed by anodic pulses. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Dubin *et al.* '821 in view of Uzoh *et al.* by applying an alternating cathodic current as taught by Dubin *et al.* '192, because Dubin *et al.* '192 teach that forward-reverse pulse plating results in voidless filling of trenches with large-grain deposits (column 8, lines 45-50).

Regarding claims 12 and 13, Dubin *et al.* '821 and Uzoh *et al.* do not teach that the step of applying a pulsed current includes a plurality of anodic pulses or that the pulses are approximately 1 sec in duration.

Dubin *et al.* '192 teach a method for plating wafers comprising forward-reverse pulsing (example 2). There are a plurality of reverse (anodic) pulses. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Dubin *et al.* '821 in view of Uzoh *et al.* by applying a plurality of anodic pulses as taught by Dubin *et al.* '192, because Dubin *et al.* '192 teach that forward-reverse pulse plating results in voidless filling of trenches with large-grain deposits (column 8, lines 45-50). Furthermore, regarding claim 13, it would have been obvious to one of ordinary skill in the art to optimize the duration of the pulses, because the length of the anodic pulse determines how much copper is etched away, and is thus a result-effective variable. See MPEP 2144.05 IIB.

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**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nira S. Birenbaum, Ph.D. whose telephone number is (571) 272-8516. The examiner can normally be reached on M-F 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King can be reached on (571) 272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

nsb

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